Nanolasers grown on silicon-based MOSFETs

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Abstract: We report novel indium gallium arsenide (InGaAs) nanopillar lasers that are monolithically grown on (100)-silicon-based functional metal-oxide-semiconductor field effect transistors (MOSFETs) at low temperature (410 °C). The MOSFETs maintain their performance after the nanopillar growth, providing a direct demonstration of complementary metal-oxide-semiconudctor (CMOS) compatibility. Room-temperature operation of optically pumped lasers is also achieved. To our knowledge, this is the first time that monolithically integrated lasers and transistors have been shown to work on the same silicon chip, serving as a proof-of-concept that such integration can be extended to more complicated CMOS integrated circuits.

OCIS codes: (250.5960) Semiconductor lasers; (160.3380) Laser materials.

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1. Introduction

Optical interconnects on silicon-based electronics offer the tantalizing prospect of cost-effectively satisfying the insatiable need for higher data speeds and lower power consumption in computing [1]. In spite of a myriad of inspiring breakthroughs in this field, integrating lasers onto silicon, thus forming indispensable on-chip light sources, still remains a major challenge. Some recent approaches have focused on directly making group IV lasers on silicon, by either taking advantage of silicon's Raman scattering effect [2–4], or engineering strain and doping concentration to improve the radiation efficiency of germanium or silicon [5]. These methods are limited by the basic fact that group IV materials have indirect bandgaps and thus provide insufficient radiation efficiency. Other researchers have turned to heterogeneous integration and bonded III-V lasers onto a silicon substrate [6–8]. However, challenging wafer bonding is usually needed to obtain an atomic level of surface flatness, causing a relatively low yield. III-V lasers monolithically grown on silicon have therefore long been an attractive goal for on-chip light sources.

Nevertheless, mismatches of both lattice constant and thermal expansion coefficient have fundamentally restricted the monolithic integration of III-V lasers onto silicon substrates. This integration is further impeded by the high growth temperature of III-V bulk materials, which damages complementary metal-oxide-semiconudctor (CMOS) chips. Recently, our group overcame these barriers and produced InGaAs-based nanopillar lasers grown on a (111)-silicon substrate using low-temperature metal-organic chemical vapor deposition (MOCVD) [9]. A novel helically-propagating mode was also proposed and simulated to explain the strong light confinement despite the low refractive index contrast between InGaAs and silicon.

Here, as a crucial further step towards on-chip integration, we report InGaAs nanopillar lasers monolithically grown on silicon-based MOSFETs. MOSFET performance is nearly the same before and after the nanopillar growth. Nanopillars grow on both the gate region (made of polycrystalline silicon) and the source/drain region (made of (100)-silicon) of the transistors at a low growth temperature of 410 °C. For the first time, room temperature optically-pumped lasers are created using nanopillars grown both on polycrystalline and (100)-crystalline silicon, attesting to the excellent crystalline quality. To our knowledge, this is the first time that monolithically integrated lasers and transistors have been shown to work on the same silicon chip. This is an important step forward for the cost-effective integration of nanopillar lasers into more complicated CMOS circuits with massive scalability.

2. Nanopillar growth on MOSFETs

We investigate the influence of III-V nanopillar growth on the MOSFET performance. Our experiments begin with a standard (100)-silicon wafer consisting of n-channel MOSFETs with various gate lengths and widths. The MOSFETs had annealed aluminum metal contacts and were fully characterized before nanopillar growth for the purposes of comparison. The metal contacts are subsequently removed from the MOSFETs by wet chemical etching, exposing the gate and source/drain regions of the transistors. The gate region consists of n-type doped polycrystalline silicon, while the source/drain region is made of n-type doped (100)-silicon. A 100-nm-thick silicon dioxide layer is then deposited onto part of the wafer to protect selected MOSFETs from III-V material deposition for the purposes of after-growth MOSFET fabrication. The wafer is loaded into the MOCVD chamber for nanopillar growth. After MOCVD growth, the silicon dioxide layer is removed and the metal contacts are evaporated onto the MOSFETs. Next, the metal contacts go through rapid thermal annealing at 350 ^{o}C for 30 seconds in a nitrogen environment. The MOSFETs and nanopillar lasers are fully characterized to confirm CMOS compatibility.

Figure 1 shows a schematic illustrating the nanopillars grown on a MOSFET. Figures 2(a) and 2(b) show scanning electron microscope (SEM) images of InGaAs/GaAs core-shell

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nanopillars grown on both the gate region and the source/drain region of the transistor. The nanopilar consists of a 630-nm-diameter InGaAs core as the active region, surrounded by a 110-nm-thick GaAs shell layer serving as a surface passivation layer. The structure and growth method are similar to those on (111)-silicon reported in [9]. What is new and most extraordinary here is the fact that micron-sized pillars are grown on polycrystalline silicon with the same core-shell structure, tapered hexagonal pillar shape, growth rate and wurzite crystalline phase. As shown in Figs. 2(a) and 2(b), nanopillars are surrounded by some III-V polycrystalline islands due to parasitic growth. Further growth condition optimization will be necessary to minimize the island formation. Alternatively, selective area growth, which has been successfully demonstrated with vapor liquid solid (VLS) nanowires [10], could be a promising approach to control the nanopillar site and remove the parasitic growth.

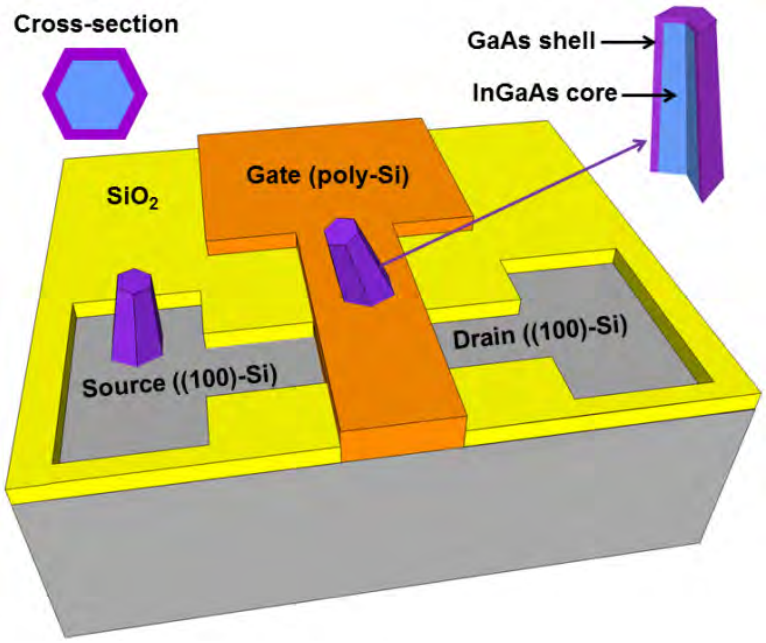

Fig. 1. Schematic of nanopillars grown on a MOSFET. Each nanopillar has a tapered hexagonal shape and consists of an InGaAs core and a GaAs shell. The nanopillars grow on both the gate and source/drain regions with a random orientation. The gate region consists of n-type doped polycrystalline silicon, while the source/drain region is made of n-type doped (100)-silicon.

The orientation of nanopillars on the gate region is random, due to multiple grain orientations inside the polycrystalline silicon. The surface of the (100)-silicon is somewhat rough as a result of the fact that the metal contacts had been annealed and then etched. As such, nanopillars on the source/drain region do not align in any particular direction. For future optimization, the metal deposition/annealing/etch step will not need to be part of the heterogeneous integration process. Under such circumstances, the nanopillars are expected to grow along the [111] crystal direction of silicon, and it will be possible to precisely control the nanopillar growth orientation on (100)-silicon substrates. As an example, we etched part of the (100)-silicon substrate to expose silicon (111) planes using an anisotropic silicon etchant (tetramethylammonium hydroxide). We show that nanopillars can grow on silicon (111) planes with a predetermined orientation. As shown in the SEM image in Fig. 2(c), a nanopillar is grown inside an inverted pyramid comprised of four degenerate silicon (111) planes, exactly following the [111] crystal direction of silicon. Although only one nanopillar

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is shown in Fig. 2(c), a density as high as 5×10^7 /cm^2 has been achieved for nanopillars on (100) silicon substrates.

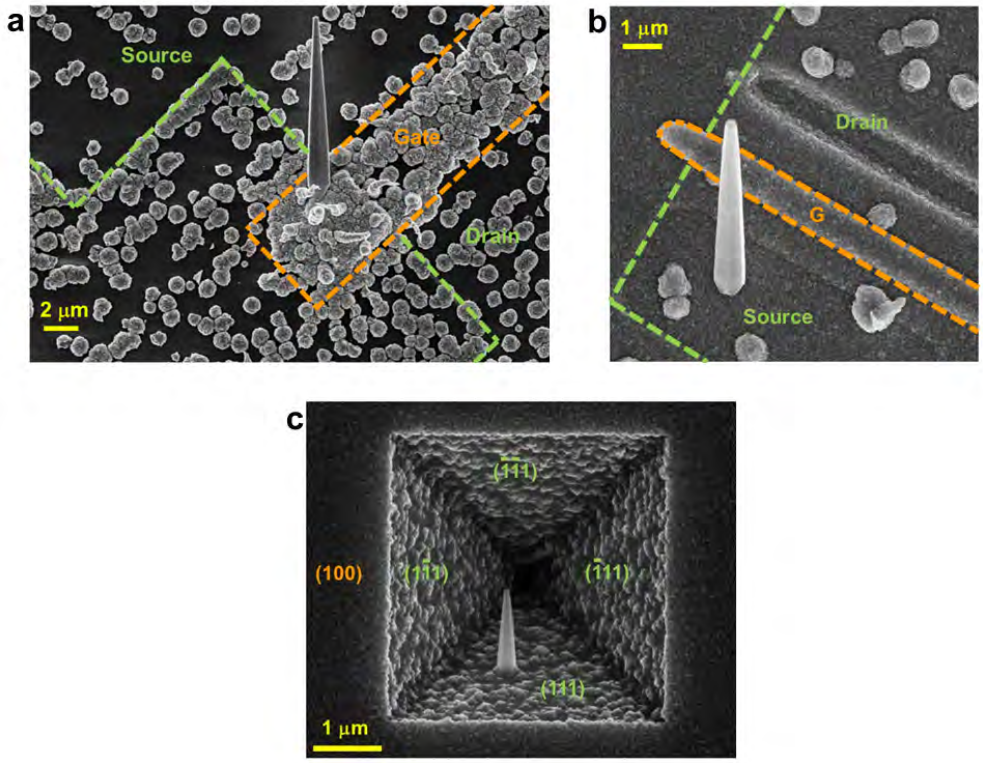

Fig. 2. SEM images of nanopillar growth. (a) The nanopillar grown on gate region (labeled Gate) of a MOSFET. (b) The nanopillar grown on source region of a MOSFET (gate region is labeled G). (c) The nanopillar grown inside an inverted pyramid on a (100)-silicon substrate. The pyramid, with four degenerate silicon (111) planes, is created by silicon anisotropic etching with tetramethylammonium hydroxide.

The growth mechanism of nanopillars on MOSFETs is believed to be initiated by spontaneous, catalyst-free nucleation of hexagonal pyramid shape nanoneedle "seeds" on a non-planar or rough surface. This is followed by layer-by-layer deposition of materials on top of the "seeds", maintaining the hexagonal shape. High indium composition abruptly stops the vertical growth [11], resulting in a hexagonal pillar shape. The nanopillar size scales with growth time. For a 1.5-hour growth time, a typical nanopillar has a base diameter of about 850 nm and a typical height of about 4 μm, as shown in Fig. 2(b). This mechanism is similar to that on (111)-silicon substrates [12–14] and more detailed investigations are underway. The growth temperature is 410 °C, making it compatible with CMOS circuits [15].

3. Nanopillar lasing characteristics

The quality of the nanopillars grown on polysilicon or the source/drain (100)-silicon is attested by the laser performance metrics. Lasing is achieved using an optical pump (120-femtosecond titanium:sapphire pulses at a wavelength of 765 nm) at room temperature. Figure 3(a) shows the laser output power as a function of pump power (L-L curve) for a typical nanopillar laser. The threshold power of 600 μW corresponds to a power density of 5.8kW/cm^2. An average output power of 0.5 μW or pulsed peak power of 573 μW is achieved. The spectra below and above threshold are shown in Fig. 3(b) with the lasing wavelength at around 980 nm (1.26 eV) and a side-mode suppression ratio of approximately

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13 dB. To evaluate the indium composition uniformity of InGaAs nanopillars, statistical micro-photoluminescence experiment has been performed over 110 nanopillars. The results show that the PL peak wavelength varies only by ± 1%, confirming the composition uniformity among nanopillars.

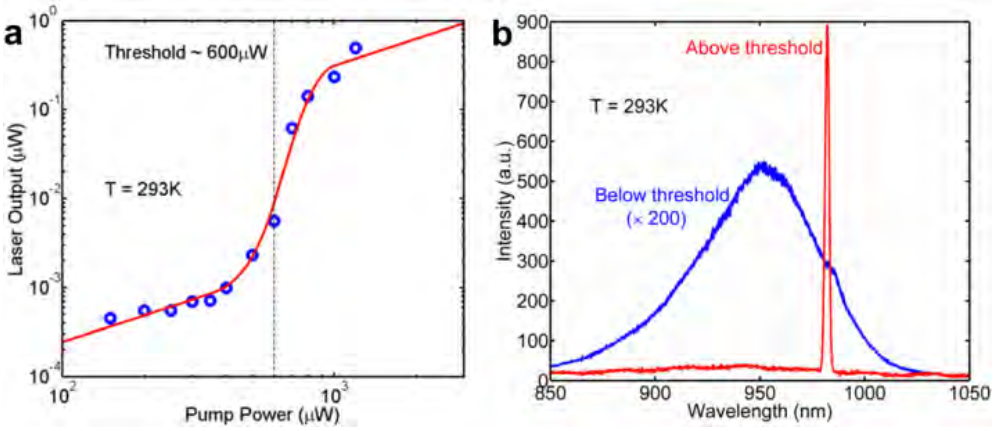

Fig. 3. Nanopillar laser oscillation. (a) L-L curve of a nanopillar laser at room temperature. The blue circles are experimental data, while the red curve is the S-shape fit. The threshold pump power is approximately 600 μW. (b) Room-temperature nanopillar emission below (blue) and above (red) threshold. For visibility, the emission below threshold is magnified by 200 times. The side mode suppression ratio of the lasing peak is about 13 dB.

4. MOSFET performance before and after nanopillar growth

The characterization of the MOSFET before and after nanopillar growth demonstrates that the growth has almost no adverse effect on the MOSFET performance. Figures 4(a) and 4(b) show typical transfer characteristics and output characteristics of a transistor before and after the nanopillar laser growth. Both I-V curves show minimal changes due to the MOCVD growth. Even after the growth, the transistor exhibits a respectable on/off current ratio of 47 dB, a subthreshold swing of approximately 140 mV per decade, and a maximum transconductance of 200 μS at a V_{ds} of 2.5 V. Systematic measurement shows that 59 out of 60 transistors offer near-constant performance after growth, resulting in a high yield of 98.3%. Statistical analysis has also been carried out on 50 transistors with the same annealing condition. Figure 4(c) shows a histogram plot of transistor threshold voltage before (dark dashed line) and after (red solid line) the nanopillar growth. On average, the threshold voltage only shifts by 3.0% after nanopillar growth.

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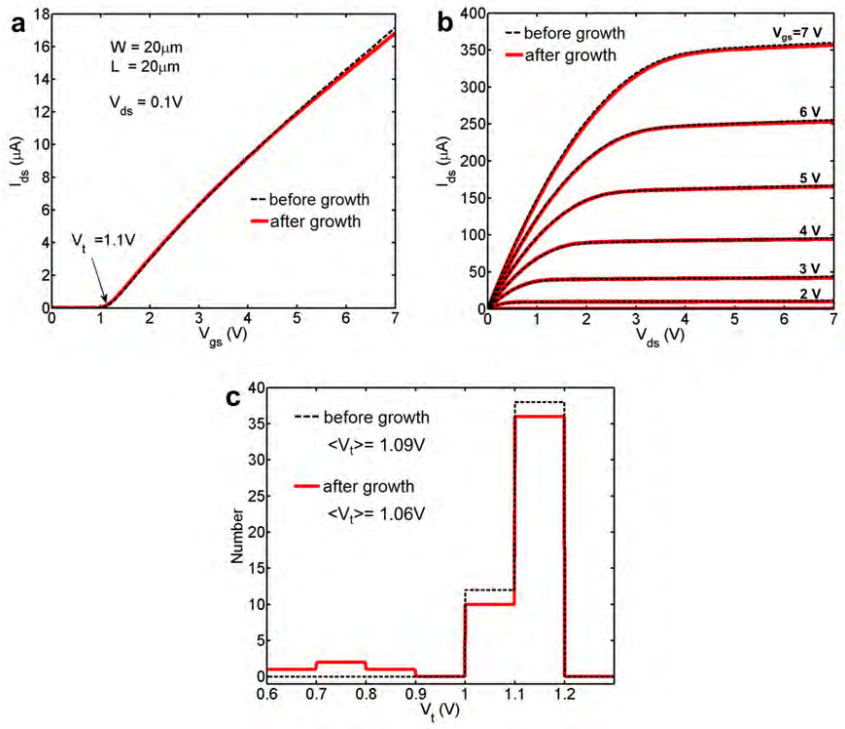

Fig. 4. Transistor performance before and after nanopillar laser growth. (a) Transfer characteristics of a transistor (gate width 20 μm, gate length 20 μm) before and after nanopillar growth. V_{gs} represents the voltage between gate and source region, and I_{ds} represents the current flowing from drain region to source region. At V_{ds} = 0.1 V, the threshold voltage is about 1.1 V. (b) Output characteristics of the same transistor before and after nanopillar growth. V_{ds} represents the voltage between drain and source region. (c) Histogram plots of the transistor threshold voltage before (dark dashed line) and after (red solid line) nanopillar growth for a sample of 50 different transistors. The average threshold voltage before growth is 1.09 V, while the average threshold voltage after growth is 1.06 V.

5. Conclusion

Using a unique low-temperature and catalyst-free nanopillar growth technique, we demonstrate the first nanolasers monolithically grown on silicon-based MOSFETs, in particular, on polycrystalline silicon. Excellent lasing performance is obtained at room temperature. The group III-V nanopillar growth process has minimal impact on the performance of the transistors, and shows great promise as a CMOS-compatible growth method. This work paves the way for the heterogeneous integration of nanophotonics, in particular lasers, directly onto silicon wafers that consist of nearly completed electronic circuits. In turn, this will open the door to a wide range of otherwise unattainable capabilities in electronic circuits, thanks to drastically reduced power consumption, weight and size.

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